BURST COUNTER CONTROLLER AND METHOD IN A MEMORY DEVICE OPERABLE IN A 2-BIT PREFETCH MODE

ABSTRACT OF THE DISCLOSURE

A burst counter generates all but the least significant bit ("LSB") of a sequence of column addresses in a 2-bit prefetch dynamic random access memory ("DRAM"). The sequence of column addresses is generated by either incrementing or decrementing the burst counter starting from an externally applied starting address. The count direction of the counter is controlled by a counter control circuit that receives the LSB the next to least significant bit ("NLSB") of the starting column address, as well as a signal indicative of the operating mode of the DRAM. In a serial operating mode, the counter control circuit causes the burst counter to increment when the LSB of the starting column address is "0" and to decrement when the LSB of the starting column address is "1". In an interleave operating mode, the counter control circuit causes the burst counter to increment when the NLSB of the starting column address is "0" and to decrement when the NLSB of the starting column address is "1".